CLAIMS

1. A wiring of a semiconductor device comprising:

a first conductive layer formed on a semiconductor substrate;

a first insulation layer formed on said first conductive layer, planarized by a CMP process and having a scratch on a surface thereof;

a second insulation layer formed on said first insulation layer;

a second conductive layer contacting said first conductive layer through a via hole formed in said first and second insulation layers; and

a third conductive layer formed in a groove formed in said second insulation layer, wherein said groove has a depth less than a thickness of said insulation layer.

2. A wiring of a semiconductor device as claimed in claim 1, wherein said first and second insulation layers are formed from a same insulation material.

3. A wiring of a semiconductor device as claimed in claim 1, wherein said second conductive layer comprises a plug filling said via hole.

4. A wiring of a semiconductor device as claimed in claim 1, wherein said first conductive layer is an impurity doped region on said semiconductor substrate.

5. A wiring of a semiconductor device as claimed in claim 1, further comprising:

a third insulation layer formed on said second insulation layer, having a second via hole therein; and

a fourth conductive layer formed on said third insulation layer, contacting said third conductive layer through said second via hole.

6. A wiring of a semiconductor device as claimed in claim 5, wherein said fourth conductive layer is a bit line formed from a conductive material selected from a group consisting of tungsten, aluminum and copper.

7. A wiring of a semiconductor device comprising:

a first conductive layer formed on a semiconductor substrate;

a first insulation layer formed on said first conductive layer, planarized by a CMP process and having a scratch on a surface thereof;

a second insulation layer formed on said first insulation layer and having a groove formed therein; and

a second conductive layer formed in said groove, having a thickness thinner than a thickness of said second insulation layer.

8. A wiring of a semiconductor device as claimed in claim 7, wherein said first and second insulation layers are formed from a same insulation material.

9. A wiring of a semiconductor device as claimed in claim 7, wherein said

second conductive layer is formed from a metal selected from a group consisting of tungsten, aluminum and copper.

10. A method of manufacturing a wiring of a semiconductor device comprising the steps of:

forming a first conductive layer on a semiconductor substrate;

forming a first insulation layer on said conductive layer by depositing a first insulating material and implementing a CMP process;

forming a second insulation layer by depositing a second insulation material on said first insulation layer in order to cover a scratch formed on said first insulation layer after implementing said CMP process;

forming an etching pattern by etching said second insulation layer to a thickness less than a thickness of said second insulation layer; and

forming a conductive pattern of a second conductive layer having a damascene shape by depositing a conductive material on said etching pattern and then planarizing the second conductive layer.

11. A method of manufacturing a wiring of a semiconductor device as claimed in claim 10, wherein said first and second insulation materials are the same.

12. A method of manufacturing a wiring of a semiconductor device as claimed in claim 11, wherein said first insulation material and said second insulation material are

silicon oxide.

13. A method of manufacturing a wiring of a semiconductor device as claimed in claim 10, wherein said first insulation material is silicon oxide.

14. A method of manufacturing a wiring of a semiconductor device as claimed in claim 10, wherein said second insulation material is silicon oxide.

15. A method of manufacturing a wiring of a semiconductor device as claimed in claim 10, further comprising a step of forming a second etching pattern by etching said first and second insulation layers.

16. A method of manufacturing a wiring of a semiconductor device as claimed in claim 10, wherein said conductive material is selected from a group consisting of tungsten, aluminum and copper.

17. A method of manufacturing a wiring of a semiconductor device as claimed in claim 10, wherein said planarizing of said conductive layer is implemented by a CMP process.